Claims

1. (Original) A method of simulating a circuit using an analog or RF simulator, comprising:

defining two circuit descriptions to be used during the simulation, a first circuit description used for accuracy of the simulation and a second circuit description, different from the first circuit description, used for increasing the speed of the simulation; and

simulating the circuit using both the first and second circuit descriptions.

2. (Currently amended) The method of claim 1, wherein the first circuit description ~~includes~~comprises parasitic information and the second circuit description has the parasitic information removed or substantially reduced.

3. (Currently amended) The method of claim 1, further ~~including~~comprising reading a netlist ~~including~~comprising parasitic information or reading a netlist and a separate file containing parasitic information, and wherein the first circuit description ~~includes~~comprises all of the elements included in the netlist plus the parasitic information.

4. (Currently amended) The method of claim 3, further ~~including~~comprising modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying ~~includes~~comprises:

analyzing values and functionality of electrical components in the circuit to determine which components are parasitic information; and

removing the parasitic information based on the analysis.

5. (Currently amended) The method of claim 3, further ~~including~~comprising modifying the first circuit description to generate the second circuit description with reduced parasitic information, wherein modifying ~~includes~~comprises:

identifying circuit components marked as parasitic information; and

removing the parasitic information based on the identification.

6. (Currently amended) The method of claim 1, wherein simulating ~~includes~~comprises solving a system of interrelated equations, wherein a part of the system of equations uses the first circuit description and wherein a part of the system of equations uses the second circuit description.

7. (Currently amended) The method of claim 1, further ~~including~~comprising:

forming a first list ~~including~~comprising circuit components without parasitic information;

forming a second list ~~including~~comprising the parasitic information;

forming first and second simulation data structures using the first and second lists, respectively; and

wherein the first circuit description is defined as a combination of the first and second lists, and the second circuit description is defined as only the first list.

8. (Currently amended) The method of claim 7, further ~~including~~comprising evaluating $F(X^i)$ using both the first and second simulation data structures for accuracy and performing a factorization of a Jacobian matrix built using only the first simulation data structure for increasing the speed of the simulation.

9. (Currently amended) The method of claim 1, wherein simulating ~~includes~~comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated equation, and ΔX is a variable to be solved, and further ~~including~~comprising factorizing the matrix J built using the second circuit description, evaluating $F(X^i)$ using the first circuit description and solving for ΔX.

10. (Original) The method of claim 1, wherein the analog simulation is used for any one or more of the following: DC, AC, and transient analysis and the RF simulation is used for state-state analysis and modulated steady-state analysis.

11. (Currently amended) The method of claim 1, wherein simulating further ~~includes~~comprises factorizing a Jacobian matrix built using the second circuit description for preconditioning a linear iterative solver.

12. (Currently amended) The method of claim 1, further ~~including~~comprising receiving, on a server computer, a circuit description from a client computer over a distributed network, simulating the description on the server computer, and returning simulation results to the client computer over the distributed network.

13 (Currently amended) An analog or RF simulator for simulating a circuit, comprising:

an elaboration engine that receives one or more lists associated with the circuit ~~including~~comprising a list of components in the circuit, interconnections between the components, and parasitic information and that defines two circuit descriptions, a first circuit description used for accuracy of the simulation and a second circuit description used for speed of the simulation, the first circuit description being different from the second circuit description; and

a simulation kernel coupled to the elaboration engine that ~~includes~~comprises at least a direct solver or linear iterative solver to simulate the circuit, wherein the simulation kernel solves a system of equations, part of the system of equations using the first circuit description and part of the system of equations using the second circuit description.

14. (Currently amended) The analog simulator of claim 13, further ~~including~~comprising a preconditioner coupled to the linear iterative solver.

15. (Currently amended) The analog simulator of claim 14, wherein the one or more lists include a netlist and a DSPF, ~~including~~comprising parasitic information.

16. (Original) The analog simulator of claim 13, wherein the simulation kernel evaluates $F(X^i)$ using the first circuit description and performs a factorization of a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$.

17. (Currently amended) The analog simulator of claim 13, further ~~including~~comprising a network coupled to the simulator through which the first circuit description is received.

18. (Currently amended) A simulator for simulating a circuit, comprising:

means for reading a first description of the circuit that ~~includes~~comprises a list of components in the circuit, the interconnections between the components, and parasitic information;

means for generating a second circuit description by removing at least a part of the parasitic information from the first circuit description; and

means for simulating the circuit using substantially the first circuit description ~~including~~comprising the parasitic information and the second circuit description with reduced parasitic information.

19. (Currently amended) The simulator of claim 18, further ~~including~~comprising means for solving a linear system of equations using an iterative solver or a direct solver.

20. (Currently amended) The simulator of claim 18, wherein the means for simulating ~~includes~~comprises evaluating $F(X^i)$ using the first circuit description and factorizing a Jacobian matrix J using the second circuit description to solve an equation $J\Delta X = -F(X^i)$.

21. (Currently amended) A method of simulating a circuit using an analog or RF simulator, comprising:

generating a system of equations wherein a part of the system of equations uses a first circuit description ~~including~~comprising parasitic information and a part of the system of equations uses a second circuit description with parasitic information removed;

solving the system of equations in order to simulate the circuit; and

outputting the simulation results.

22. (Currently amended) The method of claim 21, wherein generating the system of equations ~~includes~~comprises solving a form of the equation $J\Delta X = -F(X^i)$ wherein J is a Jacobian matrix related to the circuit components, $F(X^i)$ is an evaluated solution, and ΔX is a variable to be solved.

23. (Currently amended) The method of claim 22, wherein solving further ~~includes~~comprises factorizing the Jacobian matrix J using the modified circuit description, evaluating $F(X^i)$ using the first circuit description, and solving for ΔX.